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PATENT APPLICATION

ATTORNEY DOCKET NO. 200207083-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Blaine Stackhouse et al.

Confirmation No.: 6673

Application No.: 10/600,875

Examiner: Dang T Nguyen

Filing Date: Jun. 20, 2003

Group Art Unit: 2824

Title: Bias Generation Having Adjustable Range and Resolution Through Metal Programming

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on May 15, 2006.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 500 . At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Respectfully submitted,

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PATENT APPLICATION
ATTORNEY DOCKET NO. 200207083-1

APPEAL BRIEF dated July 6, 2006

OFFICIAL

Appl. No.	:	10/600,875	Confirmation No. 6673
Appellant	:	Blaine Stackhouse et al.	
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TC/A.U.	:	2800/2824	
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Docket No.	:	200207083-1	
Customer No.	:	022879	
Title	:	Bias Generation Having Adjustable Range and Resolution Through Metal Programming	

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APPELLANT'S BRIEF ON APPEAL

Sir:

This is an appeal under 37 CFR 41.31 from a Final Rejection in an Office Action mailed Feb. 21, 2006. A Notice of Appeal was filed on May 15, 2006 pursuant to an Advisory Action mailed April 21, 2006 and a corrected Advisory Action mailed May 18, 2006. Jurisdiction over this appeal resides in the Board of Patent Appeals and Interferences under 35 U.S.C. §134. An oral hearing was not requested.

A Certificate of Mailing or Transmission is provided on page 33 of this document and applies to this document and any Appendix attached hereto.

REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, L.P., of Houston, Texas.

RELATED APPEALS AND INTERFERENCES

Appellant is aware of no related appeals or interferences.

STATUS OF CLAIMS

Claims 1-27 are pending. Claims 12-20, 26 and 27 have been allowed and Claims 9 and 10 are objected to but deemed allowable if rewritten in independent form. The claims for consideration on appeal in the present application are Claims 1-8, 11 and 21-25. The claims on appeal are presented herewith in the attached Claims Appendix to Appeal Brief.

STATUS OF AMENDMENTS

Appellant submitted new Claims 26 and 27 in a Response/Amendment filed subsequent to final rejection. In a corrected Advisory Action mailed 5/18/06, the Examiner entered and allowed new Claims 26 and 27. There are no other, outstanding amendments for entry or consideration.

SUMMARY OF CLAIMED SUBJECT MATTER

Embodiments of the present invention facilitate a range shift or range modification and/or a resolution adjustment of a bias voltage output signal generated by a programmable weak write test mode (PWWTM) bias generator. The present invention employs metal programming to selectively add a transistor to the PWWTM bias generator during circuit manufacture. By selectively adding the transistor using metal programming, the range modifications and/or resolution adjustments are realized. A programmable bias voltage having the modified range and/or the adjustable resolution is employed to implement weak write test mode (WWTM) testing of a static random access memory (SRAM) (Page 5, Lines 20-27).

Independent Claim 1 recites, "[a] bias generator for testing of a static random access memory (SRAM)". Embodiments of the bias generator are illustrated in

Figures 1, 4 and 5, wherein the bias generator is most closely identified with reference numbers 100, 200 and 300 in the respective drawings. Various embodiments of the bias generator are generally described in Appellant's specification, for example with respect to Figure 1, at Page 5, line 28 to Page 13, line 30; with respect to Figure 4, at Page 15, line 17 to Page 17, line 21; and with respect to Figure 5, at Page 17, line 22, to Page 20, line 13. The bias generator is further characterized and defined by Appellant as a "metal-programmable weak write test mode (MPWWTM) bias generator" while SRAM testing is defined as weak-write testing. (For example, see Page 5, lines 28-29; Page 15, line 17, to Page 16, line 6; and Page 5, lines 5-27, with respect to weak-write testing).

Claim 1 further recites that the claimed bias generator comprises, "an output of the bias generator", the output being an "output signal" defined as "a bias voltage V_{bias} at an output 102" in Appellant's specification at Page 5, line 30-31. Further, Appellant specifically defines the "bias voltage V_{bias}" as having, "a magnitude that is selectable from among a set of available magnitudes" at Page 5, line 30, to Page 6, line 1. Exemplary sets of available magnitudes of the bias voltage V_{bias} are illustrated in Figures 3A-3C.

Claim 1 recites that the claimed bias generator further comprises, "means for adjusting a set of available magnitudes of a bias voltage output signal at the output using metal programming". In some embodiments, "means for adjusting" is identified or associated with operation of one or both of metal-programmable (MP) pull-up transistors 140 and MP pull-down transistors 140' illustrated in Figure 1. Additionally, "means for adjusting" is illustrated in Figure 4 as, "either or both of one or more metal-programmable (MP) pull-up transistors 240 and one or more metal-programmable (MP) pull-down transistors 240' " (Page 16, lines 9-11), and in Figure 5, as MP transistors 340, 340' (See discussion at Page 19, line 22, to Page 20, line 4).

A discussion of metal-programmable (MP) transistors 140, 140', embodiments of which are illustrated in Figures 2A and 2B, is provide at Page 7, line 29, to Page 13, line 29. Examples of an operation or action of the 'adjusting means' relative to the set of available magnitudes of a bias voltage generated by the claimed bias generator are discussed with respect to Figures 3A-3C, at Page 13, line 30 to Page 15, line 16. In particular, Figures 3A-3C illustrate that "adjusting" is defined as

modifying or shifting available values of the bias voltage V_{bias} to another set of available values. For example, as illustrated in Figure 3A, a first set "*A*" is adjusted or shifted by "means for adjusting" to produce a second set "*B*". Likewise, as illustrated in Figure 3B, the adjusting produces another set "C" while another set "D" is produced as illustrated in Figure 3C.

Independent Claim 6 recites, "[a] bias generator for testing of a static random access memory (SRAM)". Embodiments of the bias generator are illustrated in Figures 1, 4 and 5, wherein the bias generator is most closely identified with reference numbers 100, 200 and 300 in the respective drawings. Various embodiments of the bias generator are generally described in Appellant's specification as discussed above with respect to Claim 1.

Claim 6 further recites that the bias generator comprises, "a metal-programmable transistor that adjusts a set of available magnitudes of a bias voltage output signal at the bias generator output when metal programmed". The adjustment provided by the metal programmable transistor is defined by Appellant as a shift or change from one set of available magnitudes to another set, as discussed above with respect to Claim 1.

Independent Claim 21 recites, "[a] method of modifying a set of available magnitudes of a bias voltage output signal generated by a bias generator". An embodiment of the "method of modifying" recited in Claim 21 is illustrated in Figure 6, wherein the method is most closely identified with reference number 400. The method 400 of modifying is generally discussed in Appellant's specification at Page 20, line 13 to Page 22, line 23. The subject bias generator is specifically defined by Appellant as, "a programmable weak write test mode (PWWTM) bias generator" at Page 20, lines 13-23.

Claim 21 recites that the method of modifying a set of available magnitudes of a bias voltage output signal comprises, "providing a metal-programmable transistor in the bias generator" and further comprises, "metal programming the metal-programmable transistor to connect the transistor to circuitry of the bias generator, such that a corresponding ON state resistance of the metal-programmed transistor is combined with an effective ON state resistance of the circuitry to modify the available magnitudes of the set".

Specifically, an "auxiliary pull-up transistor is provided in the circuitry of the PWWTM bias generator during IC manufacture in some embodiments", the auxiliary pull-up transistor being, "provided in an isolated configuration" (Page 20, lines 26-28). The metal programming is used in "connecting 410" the provided auxiliary pull-up transistor "to circuitry of the PWWTM bias generator", according to some embodiments (Page 20, lines 24-26).

Likewise, in some embodiments, an "auxiliary pull-down transistor is provided in the circuitry of the PWWTM bias generator during IC manufacture in some embodiments", the auxiliary pull-down transistor being, "provided in an isolated configuration" (Page 21, lines 23-25). The metal programming is used in "connecting 420" the provided auxiliary pull-down transistor "to circuitry of the PWWTM bias generator" to modify available magnitudes of a bias voltage output signal, according to some embodiments (Page 21, lines 21-23).

Connecting one or both of the provided transistors using metal programming facilitates modifying or shifting values of the available magnitudes of the set. Specifically, "metal programming combines an ON state resistance of the auxiliary pull-up transistor with an effective ON state resistance of [a] pull-up transistor array [of the bias generator] to modify the available magnitudes of the generated bias voltage V_{bias}" (Page 21, lines 5-7). Similarly, "metal programming combines an ON state resistance of the auxiliary MP pull-down transistor with an ON state resistance of the pull-down transistor to modify the available magnitudes of the generated bias voltage V_{bias}" (Page 22, lines 1-3). Also see general discussion at Page 21, lines 5-20, and Page 22, lines 1-23.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Ground I: Rejection of Claims 1, 3-8, 11 and 21-25 under 35 U.S.C. 102(b) as being anticipated by Patel et al., U. S. Patent No. 6,025,737 (hereinafter 'Patel et al.').

Ground II: Rejection of Claim 2 under 35 U.S.C. 103(a) as being unpatentable over Patel et al. in further view of Ando, U. S. Patent No. 6,560,142 (hereinafter 'Ando').

ARGUMENT

For each ground of rejection that Appellant contests hereinbelow, wherein the rejection ground applies to more than one claim, the additional claims do not stand or fall together to the extent the claims are separately identified and argued below. Specifically, Appellant submits that Claims 1, 3-8, 11 and 21-25 do not stand or fall together as to the rejection under 35 U.S.C. 102(b). Separate patentability as to the respective rejections under 35 U.S.C. 102(b) and 35 U.S.C. 103(a) is explained in more detail herein below for one or both of particular claims and groups of claims.

Ground I: Rejection of Claims 1, 3-8, 11 and 21-25 under 35 U.S.C. 102(b) as being anticipated by Patel et al.

Appellant respectfully submits that the Examiner erred in making final a rejection of Claims 1, 3-8, 11 and 21-25 under 35 U.S.C. 102(b) as being anticipated by Patel et al. for failing to establish and properly support a *prima facie* case of anticipation with respect to the reference for each of the rejected claims, as detailed hereinbelow. In particular, the Examiner failed to show that Patel et al. disclose, explicitly or implicitly, "each element of the claim under consideration" (*W.L. Gore & Associates v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983)), and also failed to show that Patel et al. disclose the claimed elements "arranged as in the claim" (*Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)), as required by the Federal Circuit for *prima facie* anticipation under 35 U.S.C. 102.

Claim 1

In rejecting Claim 1 under 35 U.S.C. 102(b), the Examiner contended, 'Fig. 10C of Patel et al. discloses a bias generator [1050, 1055] for testing (intended of use) of a static random access memory", and cited Patel et al., Col. 7, lines 55-60. The Examiner further cited Col. 15, lines 48, -53, lines 50-52 and lines 62-64 of Patel et al., and contended that Patel et al. disclosed, "an output (To core) of the bias generator [1050, 1055] and means [1060, 1064] ... for adjusting a set of available magnitudes at the output of a bias voltage output signal [*sic*] (To core) at the output using metal programming". The Examiner responded to Appellant's arguments by further contending, "a bias signal is a signal uses [*sic*] to control or drive a circuit, and that

[*sic*] well understood to one [*sic*] ordinary skill in the art". The Examiner provided no source for the offered definition of "bias signal" and made no attempt to reconcile the Examiner's offered definition with the clearly different definition of "bias voltage output signal" provided by Appellant's specification. The Examiner concluded, "Patel [1050 and 1055] clearly discloses a bias signal 'To Core', because the signal 'To Core' generating [*sic*] by 1050 and 1055 is using [*sic*] to drive and control the Core; thereby 1050/1055 is a generator".

Appellant respectfully disagrees. In particular, contrary to the Examiner's contention, Patel et al. fail to disclose, explicitly or implicitly, each element of Claim 1. Patel et al. disclose neither a "bias generator" nor a "bias voltage output signal" produced at an output of the bias generator, as defined and claimed by Appellant, contrary to the Examiner's contention. Furthermore, Patel et al. do not disclose, explicitly or implicitly, "means for adjusting a set of available magnitudes", of a bias voltage, as recited in Claim 1. Similarly, Patel et al. fail to disclose or suggest a bias generator "for testing (intended of use) of a static random access memory", contrary to the Examiner's contention. In fact, the circuitry (i.e., input buffer) disclosed by Patel et al. is ***incapable*** of producing an output signal having characteristics necessary for testing static random access memory according to Appellant's definition thereof ("intended of use"). Additional discussion of intended use is provided below.

Instead, Patel et al. generally disclose circuitry for a low internal voltage integrated circuit and more particularly, "[a] technique and circuitry for interfacing an integrated circuit manufactured using technology compatible with one voltage level to other integrated circuits compatible with a different voltage level" (Patel et al., Abstract, lines 1-4). Integral to the circuitry disclosed by Patel et al. is an input buffer using an inverter circuit configuration comprising transistor 1050 and transistor 1055, "coupled in series between a positive supply and ground", which is illustrated in Figure 10B (Patel et al., Col. 15, lines 13-14). In Figure 10C and at Col. 15, lines 48-50, which are relied upon by the Examiner, Patel et al. disclose, "an example of an implementation of the input buffer in FIG. 10B using programmable metal options, such as by selecting an appropriate metal mask" (i.e., metal programming). Patel et al. further disclose, "[t]he effective size (or strength) of transistor 1050 may be adjusted using transistors 1060 and 1062 ... the effective size (or strength) of

transistor 1055 may be adjusted using transistors 1064 and 1066" (Patel et al., Col. 15, lines 50-54, further relied upon by the Examiner). An embodiment of the disclosed adjustment employs "programmable metal options" to implement using the respective transistors 1060, 1062, 1064 and 1066.

However, contrary to the Examiner's contention, Patel et al. fail to disclose, implicitly or explicitly, a "bias generator" or "an output" thereof, as defined by Appellant's specification and recited in Claim 1 (for example, see at least Appellant's specification, Page 5, line 28, through Page 6, line 9). Instead, in Figures 10B and 10C, relied upon by the Examiner, Patel et al. disclose an inverting input buffer and circuit therefor. The disclosed inverting input buffer is not equivalent to the claimed "bias generator" in either structure or function.

For example, as illustrated, the inverting input buffer receives a ***binary*** logic signal at I/O pin 820 from which an inverted ***binary*** logic output signal is produced at output 1058, labeled "To Core". The skilled artisan would recognize that the output binary logic signal "To Core" has two ***and only two*** allowed values or states (e.g., logic voltages). Moreover, the "To Core" signal, ***is and can only be*** a digital inverse of a logic level appearing on I/O pin 820 at an input of the inverting input buffer. The allowed values of the "To Core" signal are dependent only on the supply voltages VCCQ or VCCINT and VSSQ during normal operation of the inverting input buffer. In particular, a first logic level of the "To Core" signal has a voltage essentially equal to the supply voltage VCCQ, while a second logic level has a voltage essentially equal to the supply voltage VSSQ, under normal operation of the circuit according to Patel et al. Additionally, the logic level of the "To Core" signal is not 'selectable' but rather, is merely responsive to the input logic level appearing on I/O pin 820.

Hence, the inverting input buffer of Figures 10B and 10C disclosed by Patel et al., and relied upon by the Examiner, is not and cannot be equivalent to the bias generator claimed by Appellant. In particular, the inverting buffer of Patel et al. is incapable of, "producing as an output signal a bias voltage V_{bias}" having "a magnitude that is selectable from among a set of available magnitudes", as defined by Appellant for the bias generator recited in the claims (Appellant's specification, Page 5, line 30, through Page 6, line 1). Except for the metal programmability, the inverting input buffer disclosed by Patel et al. is a conventional buffer known in the art and entirely

unrelated to the bias generator recited in Appellant's Claim 1. Conventional buffer circuits are recognized as being different and distinct from bias generators by the skilled artisan as can be confirmed by consulting essentially any basic textbook on electronics.

Furthermore, the Examiner's contention, "a bias signal is a signal uses [*sic*] to control or drive a circuit", is incompatible with the clearly different definition of "bias voltage output signal" provided in Appellant's specification. Specifically, Appellant submits that the Examiner erred in disregarding Appellant's clear and consistent definition and usage of the claim terms, "bias generator" and "bias voltage output signal" in the specification, as originally filed. It is well established that the Examiner may not simply fabricate and subsequently employ, without explicit support in the prior art, any definition of Appellant's claim terms that may advantageously provide support to the Examiner's rejection. In particular, in establishing a *prima facie* case of anticipation, "the trier of fact must identify the elements of the claims, ***determine their meaning in light of the specification and prosecution history***, and identify corresponding elements disclosed in the allegedly anticipating reference." (***emphasis*** added) *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, cited *supra*.

Moreover, as stated in the MPEP §2173.01, "[a] ***fundamental*** principle contained in 35 U.S.C. 112, second paragraph is that applicants are their own lexicographers. They can define in the claims what they regard as their invention essentially in whatever terms they choose so long as any special meaning assigned to a term is clearly set forth in the ***specification***" (***emphasis*** added). Additionally, "[c]onsistent with the well-established axiom in patent law that a patentee or applicant is free to be his or her own lexicographer, a patentee or applicant may use terms in a manner contrary to or inconsistent with one or more of their ordinary meanings if the written description clearly redefines the terms. See, e.g., *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999)" (MPEP §2173.05(a)(III)).

Thus, during examination, while the claims must be interpreted as broadly as their terms reasonably allow, it is not only permissible but often necessary for the Examiner to use definitions from the specification for terms appearing in the claims in

order to properly interpret claim language (see MPEP §2111.01). Furthermore, "[w]here an ***explicit definition is provided*** by the applicant for a term, that definition ***will control interpretation*** of the term as it is used in the claim. *Toro Co. v. White Consolidated Industries Inc.*, 199 F.3d 1295, 1301, 53 USPQ2d 1065, 1069 (Fed. Cir. 1999) (***emphasis*** added)" MPEP, 2111.01 *Plain Meaning*, Part III. Thus, the Examiner is obliged to employ Appellant's definition of claim terms when an explicit definition is provided pursuant to Appellant's statutory right to be his/her own lexicographer (*Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, cited *supra*).

Regarding the Examiner's particular definition of the term "bias voltage", a more common and consistent definition of the term is a voltage (typically DC) applied to a component or device to establish a reference level or operating point of the device. More particularly, as employed in weak write testing of a static random access memory (SRAM), the term "bias voltage" specifically applies to a programmable voltage that, "facilitates adjusting or modulating a strength of the weak write pull-down transistor". The bias voltage compensates, "for manufacturing related variations in a performance of the weak write pull-down transistor", as provided in the instant patent application (Appellant's specification, Page 5, lines 17-19).

In contrast, the "To Core" signal according to Patel et al. is neither a programmable voltage nor a voltage that is applied to a component or device to establish a reference level or operating point of the device. Also, in the inverter input buffer circuit (i.e., 1050, 1055) according to Patel et al., the "To Core" signal may take on either of two predetermined (but not programmable) voltages, the voltage being entirely determined by the supply voltages VCCQ or VCCINT and VSSQ applied to the circuit, as noted above. Moreover, the inverter input buffer, according to Patel et al., does not 'bias' a component or device with the "To Core" signal but merely acts as a data interface that passes digital data from the I/O pin 820 to a core of the integrated circuit. As such, the Examiner conclusion, "Patel [1050 and 1055] clearly discloses a bias signal 'To Core', because the signal 'To Core' generating [*sic*] by 1050 and 1055 is using [*sic*] to drive and control the Core; thereby 1050/1055 is a generator" is respectfully without merit.

Further, Patel et al. do not disclose, explicitly or implicitly, "means for adjusting a set of available magnitudes of a bias voltage output signal at the output using metal programming", as recited, in part, in Claim 1. In particular, according to Patel et al. at Col. 15, lines 28-29, "the input threshold trip point of the inverter may be programmable" (i.e., programmable using "metal options" associated with transistors 1060, 1062, 1064, and 1066). Also see Patel et al., Col. 15, lines 48-53. As employed by Patel et al., "trip point of the inverter" has its normal and customary meaning in the art (i.e., a voltage level at the I/O pin 820 at which the binary logic output signal at output 1058 transitions from one logic level to another). At Col. 15, lines 29-31, Patel et al. further disclose, "[t]he input threshold trip point depends on the ratio of the relative ***strengths*** of the ratio of the pull-up transistor 1050 to the pull-down transistor 1055" (***emphasis*** added). According to Patel et al., "[t]he effective size (or strength) of transistor 1050 may be adjusted by using transistors 1060 and 1062," while "the effective size (or strength) of transistor 1055 may be adjusted using transistors 1064 and 1066" (Patel et al., Col. 15, lines 50-54). As such, Patel et al. clearly disclose programming or "adjusting" the ***input threshold trip point*** of the inverting buffer circuit. However, Patel et al. do not disclose "means for adjusting" an output signal or, more specifically, "a set of available magnitudes of a bias voltage output signal at the output", as recited in Claim 1 by Appellant.

In other words, while Patel et al. may disclose "adjusting", the only adjusting disclosed is of the input threshold trip point. However, the input threshold trip point has ***no effect*** on a non-transient output voltage produced by the inverting buffer circuit. Specifically, the adjustment disclosed by Patel et al. does not change or adjust a voltage of either or both of the two logic levels produced by the inverting buffer circuit at an output. In short, the disclosed "metal options" ***do not*** and cannot affect a level of an output signal (e.g., "To Core") of the inverting buffer according to Patel et al. Thus, Patel et al. clearly do not disclose, "means for adjusting a set of available magnitudes of a bias voltage ***output*** signal," as recited in Claim 1 (***emphasis*** added).

In fact, Patel et al. explicitly recognize that the "metal options" or metal programming do not affect the magnitudes of the voltages associated with the binary output signal of the disclosed inverter. As discussed above, Patel et al. clearly state that the metal options are employed to adjust the size of the transistors 1050, 1055,

and thereby produce an adjustment in the trip point of the inverting input buffer, and ***nothing more*** is expressly stated or implied. Thus, for the Examiner to contend that Patel et al. disclose, "adjusting ... bias voltage output signal at the output" of the bias generator, or anything that is remotely similar thereto, is respectfully incorrect in light of the prior art disclosure and is entirely without merit. The "metal options" of Patel et al. simply ***do not and cannot*** adjust an output voltage of the inverting input buffer, contrary to the Examiner's contentions.

Finally, the Examiner is respectfully incorrect that, at Col. 7, lines 55-60, "Patel et al. discloses a bias generator [1050, 1055] for testing (intended of use) of a static random access memory SRAM". In fact, at Col. 7, lines 55-60, Patel et al. merely disclose, "[t]here are many techniques for implementing the programmable options feature of the present invention ..." and specifically mentions that the programmable options, "include, and are not limited to, laser programmable options, fuses, antifuses, ... EEPROM, Flash EPROM, and SRAM, and many others". As such, contrary to the Examiner's contention, Patel et al. are disclosing approaches for implementing "programmable options" wherein the options may include using SRAM. However, neither at Col. 7, lines 55-60, nor anywhere else therein, do Patel et al. disclose or even suggest, "testing a static random access memory (SRAM)", or a bias generator therefor. The word 'test' or its many art-recognized variants never appears in the disclosure of Patel et al. Thus, the Examiner respectfully cannot properly contend that Patel et al. disclose or even suggest a bias generator for testing SRAM.

That notwithstanding, the Examiner contended, "the word 'test' is an intended of [*sic*] use because a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from prior art apparatus satisfying the claimed structural limitations".

Appellant respectfully points out that, regardless of the 'intended use', for the reasons set forth above, the disclosure by Patel et al. is far from being a "prior art apparatus satisfying the claimed structural limitations", as contended by the Examiner. However, while not depending on a "use" of the claimed bias generator to distinguish over the structure of Patel et al., Appellant firmly believes that the use (i.e., functional language) actually does place meaningful limitations on the bias generator that are consistent with both the letter and spirit of 35 U.S.C. 112. In

particular, functional language used, "to define a particular capability or purpose that is served by the recited element", in a way that sets, "definite boundaries on the patent protection sought", is perfectly acceptable claim language that must be considered. (See MPEP §2173.05(g)). Not only is the inverting input buffer of Patel et al. not used for testing SRAM, the inverting input buffer ***cannot be employed as a bias generator for such testing*** where the testing is 'weak write testing', as defined in Appellant's specification.

In particular, electronic circuits are generally well-behaved and predictable or they would lack particular utility. Thus, a structure of a given electronic circuit determines what output signals that circuit can and cannot produce. When two circuits are incapable of producing the same or substantially similar output signals, those two circuits cannot be considered equivalent regardless of an intended usage thereof. As such, for structural equivalence to be established when "testing" is claimed, a hypothetical circuit that may appear in a prior art reference at least must be inherently capable of producing an output signal that is useful for the claimed testing, even if such intended use for testing is not explicitly recognized by the reference. With out such an inherent capability of the structure, the hypothetical circuit cannot be equivalent or even similar to the claimed structure.

As discussed above, the inverter input buffer is singularly ***incapable*** of producing an output signal that meets the criteria for weak write testing of SRAM according to Appellant's definition thereof. The absence of such a capability, in and of itself, precludes equivalence and, by extension, obviates any discussion of alleged anticipation by that circuit. Thus, contrary to the Examiner's contention, testing SRAM can and, in this case, does structurally distinguish the claimed bias generator from the inverting input buffer according to Patel et al. simply by establishing capabilities of the claimed bias generator. The inverting input buffer is clearly not equivalent or even remotely similar to the bias generator claimed by Appellant at least since it is incapable of being used for weak write testing of SRAM. Thus, reference to testing SRAM using Appellant's claimed bias generator does, in fact, place meaningful structural (e.g., capability) limitations on the bias generator.

Therefore for at least the reasons discussed above, Patel et al. lack implicit or explicit disclosure of 'each and every element', and further lack disclosure of such

elements 'arranged as in the claim' that are recited in Appellant's Claim 1, as required for establishing *prima facie* anticipation. *W.L. Gore & Associates v. Garlock*, cited *supra* and *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, cited *supra*. In particular, as detailed above, the Examiner failed to show that there is, "no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention," as required by the Federal Circuit. *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 USPQ 2d 1001, 1010 (Fed. Cir. 1991). Hence, a *prima facie* case of anticipation with respect to Claim 1 in view of Patel et al. has not been and respectfully cannot be established.

Claims 3-5 as dependent from Claim 1

Claims 3-5 are ultimately dependent from and include all of the limitations of base Claim 1. Having failed to establish *prima facie* anticipation of base Claim 1 with respect to Patel et al., the Examiner has similarly failed to establish *prima facie* anticipation of Claims 3-5 that are dependent therefrom for at least the same reasons given above regarding Claim 1.

Claim 3 Standing Alone

In rejecting Claim 3 under 35 U.S.C. 102(b), the Examiner contended, "Fig. 10C [of Patel et al.] further discloses wherein the means for adjusting [1060, 1064] comprise a metal [programmable] transistor (Col. 15 lines 48-53) in the bias generator [1050, 1055] ... that change one or both of a range and a resolution of the set of available magnitudes (To core) when the metal programmable transistors [1060, 1064] is metal programmed (Fig. 10D, 10E)".

Contrary to that contended by the Examiner, Patel et al. neither disclose 'each element or limitation' of Claim 3 nor the elements/limitations 'arranged as in the claim', as required by the Federal Circuit (*W.L. Gore & Associates v. Garlock*, cited *supra* and *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, cited *supra*). In particular, notwithstanding that Patel et al. fail to disclose, explicitly or implicitly, either a "bias voltage" or "means for adjusting" the bias voltage, as claimed by Appellant (see discussion above with respect to Claim 1), Patel et al. clearly fail to disclose, "wherein the means for adjusting comprises a metal-programmable transistor ... that change one or both of a range and a resolution of the

set of available magnitudes when the metal-programmable transistor is metal programmed", as recited in Claim 3 by Appellant.

As discussed above, the only metal programmable transistors (e.g., 1060, 1062, 1064, 1066) disclosed by Patel et al. are employed to effect changes in or "fine-tune" the ***input threshold trip point*** of the inverting buffer circuit (See Patel, Col. 15, line 28-61). Patel et al. fail to disclose, explicitly or implicitly, using metal programmable transistors for any other purpose beyond the aforementioned "fine-tuning". Moreover, even absent such a disclosure, transistors 1060, 1062, 1064 and 1066 do not and cannot affect changes in a magnitude of a signal output by the inverting buffer circuit. Since transistors 1060, 1062, 1064 and 1066 do not affect a level of the "To core" signal, Patel et al. do not and respectfully cannot disclose using a metal-programmable transistor to, "change one or both of a range and a resolution of the set of available magnitudes", of the inverting buffer circuit output signal (e.g., "To core"). Furthermore, Patel et al. never disclose another means for adjusting one or both of a range and a resolution of the set of available magnitudes of the output signal (e.g., "To core") of the inverting input buffer circuit. Thus, Patel et al. fail to disclose, explicitly or implicitly, each element or limitation recited in Appellant's Claim 3.

As such, the Examiner failed to show with respect to Claim 3 that Patel et al. disclose, explicitly or implicitly, 'each and every element' and further did not show that Patel et al. disclose each element 'arranged as in the claim', as required for establishing *prima facie* anticipation. *W.L. Gore & Associates v. Garlock*, cited *supra* and *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, cited *supra*. Therefore, a *prima facie* case of anticipation with respect to Claim 3 in view of Patel et al. has not been established or properly supported.

Claim 4 Standing Alone

In rejecting Claim 4 under 35 U.S.C. 102(b), the Examiner contended, "Fig. 10C et al. further comprising: a pull-up array of transistor [1062 ...] connected between a first supply voltage [VCCQ] and the bias generator output (To core); a pull-down transistor [1066 ...] connected between the bias generator output (To core) and a second supply voltage [GROUND]; and a gate bias circuit (Fug [*sic*], 10E [shift trip point down]) connected between a mode select input (Fig. 10E [Pin]) and a gate of the pull-down transistor [1064], wherein the metal-programmable pull-up transistor

[1060] is connectable in parallel or in series with the pull-up transistor array [1062 ...], and wherein the metal-programmable pull-down transistor [1064] is connectable in parallel or in series with the pull-down transistor [1064 ...]".

The Examiner appears to be equating: the transistors "[1062 ...]" and presumably 1060 of Patel et al., Fig. 10C, with Appellant's "pull-up array of transistors", and the transistors "[1066 ...]" and presumably transistor 1064 of Patel et al., Fig. 10C, with Appellant's "pull-down transistor". Further, the Examiner appears to be equating a circuit illustrated in Patel et al., Fig. 10E, comprising transistors 1050, 1055 connected as an inverting buffer, and pull-down transistors 1064, 1066, connected in parallel with transistor 1055, as being equivalent to Appellant's "gate bias circuit", recited in Claim 4. In addition, the Examiner appears to equate "PIN" (e.g., "I/O pin 820", Fig. 10B) that functions as (i.e., physical input) or is an input (i.e., an input signal) to the disclosed inverting buffer circuit with "a mode select input", recited in Claim 4. The Examiner further appears to equate transistor 1060 of Patel et al. with Appellant's claimed "metal-programmable pull-up transistor", while transistor 1064 of Patel is apparently considered equivalent to both the "pull-down transistor" and the "metal-programmable pull-up transistor", recited in Claim 4.

Note that Patel et al. make no distinction whatsoever between transistors 1060 and 1062, etc. (i.e., 1060, 1062, ..." in Fig. 10C) except that each of these transistors may have different relative sizes and may be optionally and presumable individually connected to the circuit through metal programming to adjust an effective size of transistor 1050 (See Patel et al., Col. 15, line 48-61). Similarly, Patel et al. also make no distinction between transistors 1064 and 1066, etc. (i.e., 1064, 1066, ..." in Fig. 10C) except for their respective optional connection to effect changes in the size of the transistor 1055 (See Patel et al., cited *supra*).

However, contrary to the Examiner's contention, Patel et al. fail to disclose, explicitly or implicitly, 'each element or limitation' and 'each element arranged as in' Claim 4. Specifically, Patel et al. disclose transistors 1060, 1062, etc., as "programmable metal options" for adjusting the effective size of transistor 1050. As such, the Examiner is not at liberty to separately equate the transistor 1060 (of the programmable metal options) to Appellant's "metal programmable pull-up transistor" while arbitrarily equating transistors "[1062 ...]" (of the programmable metal options)

with the Appellant's "pull-up array of transistors" of Claim 4. Patel et al. treat the programmable metal option transistors 1060, 1062, etc. as equivalent with respect their function and effect in the inverting buffer circuit. Therefore, there is no support in the Patel et al. reference teachings of separate and distinct functionality of the respective transistors, as apparently contended by the Examiner. Similarly, there is no evidence of record that transistors 1060, 1062, etc. have or may have functionality with respect to the inverting input buffer circuit that is different from that specifically disclosed by Patel et al. As such, the Examiner may not assign different and distinct functions to these transistors merely to support the rejection of Claim 4.

That notwithstanding, Appellant defines the "pull-up array of transistors" as having "a set of selection inputs Sel_i" connected to allow, "one or more of the array transistors to be selectively activated or 'turned ON' by asserting one or more of the selection inputs Sel_i" (Appellant's specification, Page 6, line 31 to Page 7, line 2). Clearly, the alleged transistors "[1062 ...]" lack any such set of selection inputs according to Patel et al. Moreover, according to Appellant's definition, the pull-up array of transistors provides selection of particular magnitudes of the bias generator output signal from among the set of available magnitudes through selective activation of transistors in the array (See for example, Appellant's specification, Page 11, lines 1-18). Since it has been established above that the transistors 1060, 1062 cannot effect a magnitude of the output signal of the inverting buffer circuit of Patel et al. and further established above that transistors "[1062, ...]" lack any sort of selection input, then transistors "[1062, ...]" are not and cannot be equivalent to the "pull-up array of transistors" recited in Claim 4 by Appellant.

Furthermore, the transistor 1066 of Patel et al. is not equivalent to "the pull-down transistor" defined and claimed by Appellant. In particular, according to Patel et al., the transistor 1066 along with transistor 1064 are programmable metal option transistors used to modify an effective size of transistor 1055 (Patel et al., Col. 15, lines 48-61). Appellant clearly distinguishes between a metal programmable pull-down transistor and the aforementioned "pull-down transistor" as separate transistors recited in Claim 4. Moreover, Appellant clearly defines the claimed "pull-down transistor" as being activated and inactivated by a "a gate bias voltage V_g" applied to a gate of the pull-down transistor, the gate bias voltage V_g being controlled by a mode

select *MS* input (See Appellant's specification, Page 7, line 9-22). Patel et al. do not provide for such activation or inactivation of transistor 1066 and fail to distinguish between transistors 1064 and 1066. Thus, transistor 1066 is not equivalent to the "pull-down transistor", as recited in Claim 4.

Assuming *arguendo* that transistor 1066 of Patel et al. is a pull-down transistor, then the inverting buffer circuit illustrated in FIG. 10E of Patel et al. is not and cannot be equivalent to Appellant's "gate bias circuit", recited in Claim 4. In particular, the "gate bias circuit" is "connected between a mode select input and a gate of the pull-down transistor", as recited in Claim 4. However, the inverting buffer circuit illustrated in FIG. 10E of Patel et al. comprises transistor 1066 and thus cannot be connected between the mode select input and the transistor. Furthermore, the "gate bias circuit" provides a signal that activates or inactivates the "pull-down transistor" according to Appellant's clear definition in the specification at Page 7, lines 9-28. Patel et al. do not provide such a circuit in FIG. 10E or in their disclosure taken as a whole. Moreover, Patel et al. fail to disclose or even suggest a "mode select input". Thus, Patel et al. clearly lack disclosure of "a gate bias circuit", as recited in Claim 4.

Finally, the Examiner may not use the same element disclosed by Patel et al. to serve as two distinctly different elements that are separately recited in Appellant's claim. Specifically, transistor 1064 cannot be equivalent to both the "metal-programmable pull-down transistor" and separately to the "pull-down transistor", which are separately recited in Claim 4. Looked at in another way, it is not possible to connect transistor 1064 in parallel or in series with itself.

As such, the Examiner failed to show with respect to Claim 4 that Patel et al. disclose, explicitly or implicitly, 'each and every element' and further did not show that Patel et al. disclose each element 'arranged as in the claim', as required for establishing *prima facie* anticipation. *W.L. Gore & Associates v. Garlock*, cited *supra* and *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, cited *supra*. Therefore, a *prima facie* case of anticipation with respect to Claim 4 in view of Patel et al. has not been established or properly supported.

Claim 5 Standing Alone

In rejecting Claim 5 under 35 U.S.C. 102(b), the Examiner contended, "Fig. 10C et al. further discloses wherein each of the metal-programmable pull-up transistor and

the metal-programmable pull-down-transistor [1060, 1064] has a respective ON state resistance ... to adjust the set of available magnitudes".

Contrary to the Examiner's contention, Patel et al. fail to disclose 'each element or limitation' and 'each element arranged as in' Claim 5. Specifically, transistors 1060, 1062, 1064, and 1066, etc. do not and cannot affect a magnitude of the output signal "To core" produced by the inverting buffer circuit according to Patel et al., as discussed above. Therefore, Patel et al. fail to disclose metal programmable pull-up and pull-down transistors, wherein effective ON state resistances thereof, "adjust the set of available magnitudes" when metal programmed, as recited in Claim 5, contrary to that contended by the Examiner.

Hence, the Examiner failed to show with respect to Claim 5 that Patel et al. disclose, explicitly or implicitly, 'each and every element' and further did not show that Patel et al. disclose each element 'arranged as in the claim', as required for establishing *prima facie* anticipation. *W.L. Gore & Associates v. Garlock*, cited *supra* and *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, cited *supra*. Therefore, a *prima facie* case of anticipation with respect to Claim 5 in view of Patel et al. has not been established or properly supported.

Claim 6

In rejecting independent Claim 6, the Examiner contended, "Fig. 10C of Patel et al. discloses a bias generator [1050, 1055] for testing (intended of use) of a static random access memory SRAM (Col. 7 lines 55-60) comprising: a metal programmable transistor [1060, 1064] that adjusts a set of available magnitudes of a bias voltage output signal (To Core) at the bias generator output (output of 1050, 1055) when metal programmed (Fig. 10D, 10E)".

Appellant respectfully disagrees. In particular, contrary to the Examiner's contention, Patel et al. fail to disclose, explicitly or implicitly, each element of Claim 6 and therefore, cannot disclose the elements of Claim 6 arranged as in the claim. For example, Patel et al. disclose neither a "bias generator" nor a "bias voltage output signal" produced at an output of the bias generator, as claimed by Appellant, contrary to the Examiner's contention. Similarly, Patel et al. fail to disclose or suggest a bias generator, "for testing (intended of use) of a static random access memory", contrary to the Examiner's contention. In fact, the circuitry (i.e., input buffer) disclosed by

Patel et al. is ***incapable*** of producing an output signal having the necessary characteristics for testing static random access memory according to Appellant's definition (i.e., "intended of use"). The incapability of the inverting input buffer circuit of Patel et al. to be employed to produce an output signal, as defined by Appellant, in and of itself precludes anticipation of Claim 6 by the Patel et al. reference.

That notwithstanding, Patel et al. further do not disclose, "a metal-programmable transistor that adjusts a set of available magnitudes of a bias voltage output signal at the bias generator output when metal programmed", as recited in Claim 6. Instead, Patel et al. disclose "metal options" or metal programmable transistors (i.e., transistors 1060, 1062, 1064, and 1066) for adjusting an ***input threshold trip point*** of an inverting input buffer (See Patel et al. Col. 15, lines 28-67). Moreover, the only effect that "selecting an appropriate metal mask" has or can reasonably be expected to have on the disclosed inverting input buffer circuit is to "fine-tune the input threshold trip point", according to Patel et al. (see Patel et al., Col. 15, lines 48-61). As disclosed by Patel et al., transistors 1060, 1062, 1064 and 1066 do not and cannot affect a magnitude of an output voltage or signal (e.g., "To Core") of the inverting input buffer, as apparently contended by the Examiner. Hence, the Examiner is respectfully incorrect in contending that the "metal options" associated with the programmable input threshold trip point of Patel et al. are, or reasonably could be, the claimed, "metal-programmable transistor that adjusts a set of available magnitudes of a bias voltage output signal," as recited in Appellant's Claim 6. Furthermore, Patel et al. disclose no other metal programmable transistors beyond transistors 1060, 1062, 1064, and 1066, which may be employed to adjust a set of available magnitudes of an output signal.

Hence, the Examiner failed to show with respect to Claim 6 that Patel et al. disclose, explicitly or implicitly, 'each and every element' and further did not show that Patel et al. disclose each element 'arranged as in the claim', as required for establishing *prima facie* anticipation. *W.L. Gore & Associates v. Garlock*, cited *supra* and *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, cited *supra*. Therefore, a *prima facie* case of anticipation with respect to Claim 6 in view of Patel et al. has not been established or properly supported.

Claims 7-8 and 11 as dependent from Claim 6

Claims 7-8 and 11 are ultimately dependent from and include all of the limitations of base Claim 6. Having failed to establish *prima facie* anticipation of base Claim 6 with respect to Patel et al., the Examiner has similarly failed to establish *prima facie* anticipation of claims that are dependent therefrom for at least the same reasons given above regarding Claim 6.

Claim 7 Standing Alone

In rejecting Claim 7 under 35 U.S.C. 102(b), the Examiner contended, "the claims [i.e., Claims 7 and 8] incorporated the same subject matter as of [*sic*] claims 3 and 4, and rejected [*sic*] along the same rationale".

However, contrary to the Examiner's contention, Patel et al. fail to disclose 'each element or limitation' and 'each element arranged as in' Claim 7 standing alone. Specifically, Patel et al. disclose transistors 1060, 1062, etc., as "programmable metal options" for adjusting the effective size of transistor 1050. Therefore, the Examiner is not at liberty to equate the "programmable metal option" transistor 1060 to Appellant's "metal programmable pull-up transistor" while arbitrarily and separately equating "programmable metal option" transistors "[1062 ...]" with the separately recited "pull-up array of transistors" in Claim 7. Since Patel et al. treat the programmable metal option transistors 1060, 1062, etc., as equivalent with respect their function and effect in the inverting buffer circuit (see discussion above with respect to Claim 4, for example), there is no support in the Patel et al. reference teachings of separate and distinct functionality of the respective "programmable metal option" transistors. Similarly, there is no evidence of record that transistors 1060, 1062, etc. have or may have functionality with respect to the inverting input buffer circuit that is different from that specifically disclosed by Patel et al. As such, the Examiner may not arbitrarily assign different and distinct functions to these transistors merely to support the rejection of Claim 7.

That notwithstanding, as noted above, Appellant defines the "pull-up array of transistors" as having "a set of selection inputs Sel_i" that allow, "one or more of the array transistors to be selectively activated or 'turned ON' by asserting one or more of the selection inputs Sel_i" (Appellant's specification, Page 6, line 31 to Page 7, line 2). Clearly, transistors "[1062 ...]" disclosed by Patel et al. lack any such set of selection

inputs. Thus, transistors "[1062, ...]" are not and cannot be equivalent to the "pull-up array of transistors" recited in Claim 7.

Moreover, the pull-up array of transistors, according to Appellant's definition, provides selection of particular magnitudes of the bias generator output signal from among the set of available magnitudes through selective activation of transistors in the array (See for example, Appellant's specification, Page 11, lines 1-18). Additionally, since it has been established above that the transistors 1060, 1062 cannot effect a magnitude of the output signal of the inverting buffer circuit of Patel et al., then transistors "[1062, ...]" are not and cannot be equivalent to the "pull-up array of transistors" claimed by Appellant.

Furthermore, the transistor 1066 of Patel et al. is not equivalent to "the pull-down transistor", defined and claimed by Appellant and discussed above with respect to Claim 4. Likewise, contrary to that contended by the Examiner, transistor 1064 of Patel et al. is not and cannot be equivalent to ***both*** the "metal-programmable pull-down transistor" and the separately recited "pull-down transistor" in Claim 7 (i.e., transistor 1064 cannot be connected in parallel or in series with itself). Moreover, contrary to the Examiner's contention, Patel et al. lack a disclosure of "a gate bias circuit", as recited in Claim 7.

As such, the Examiner failed to show with respect to Claim 7 that Patel et al. disclose, explicitly or implicitly, 'each and every element' and further did not show that Patel et al. disclose each element 'arranged as in the claim', as required for establishing *prima facie* anticipation. *W.L. Gore & Associates v. Garlock*, cited *supra* and *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, cited *supra*. Therefore, a *prima facie* case of anticipation with respect to Claim 7 in view of Patel et al. has not been established or properly supported.

Claim 8 Standing Alone

In rejecting Claim 8 under 35 U.S.C. 102(b), the Examiner contended, "the claims [i.e., Claims 7 and 8] incorporated the same subject matter as of claims 3 and 4, and rejected [*sic*] along the same rationale".

Contrary to that contended by the Examiner, Patel et al. neither disclose each element or limitation of Claim 8 nor disclose the elements 'arranged as in the claim'. In particular, Patel et al. fail to disclose either a "bias voltage" or "a metal

programmable transistor that adjusts" the bias voltage, as claimed by Appellant. In addition, Patel et al. clearly fail to disclose, "wherein the metal-programmable transistor comprises either or both of a metal-programmable pull-up transistor and a metal-programmable pull-down transistor ... the metal-programmable transistor changing one or both of a range and a resolution of the set of available magnitudes when the metal-programmable transistor is metal programmed", as recited in Claim 8.

As discussed above, the only metal programmable transistors (e.g., 1060, 1062, 1064, 1066) disclosed by Patel et al. are employed to effect changes in or "fine-tune" the ***input threshold trip point*** of the inverting buffer circuit (See Patel, Col. 15, line 28-61). Transistors 1060, 1062, 1064 and 1066 do not and cannot affect changes in a magnitude of a signal output by the inverting buffer circuit. Since transistors 1060, 1062, 1064 and 1066 do not affect a level of the "To core" signal, Patel et al. do not and respectfully cannot disclose using a metal-programmable transistor to, "change one or both of a range and a resolution of the set of available magnitudes", of the inverting buffer circuit output signal (e.g., "To core"), contrary to that contended by the Examiner. Moreover, Patel et al. never disclose another means for adjusting or changing one or both of a range and a resolution of the set of available magnitudes of the output signal. Thus, Patel et al. fail to disclose, explicitly or implicitly, each element or limitation recited in Claim 8.

As such, the Examiner failed to show with respect to Claim 8 that Patel et al. disclose, explicitly or implicitly, 'each and every element' and further did not show that Patel et al. disclose each element 'arranged as in the claim', as required for establishing *prima facie* anticipation. *W.L. Gore & Associates v. Garlock*, cited *supra* and *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, cited *supra*. Therefore, a *prima facie* case of anticipation with respect to Claim 8 in view of Patel et al. has not been established or properly supported.

Claim 21

In rejecting independent Claim 21, the Examiner contended, "Fig. 10C of Patel et al. discloses a method of modifying a set of available magnitudes (Col. 15 lines 50-55) of a bias voltage output signal [To Core] generated by a bias generator" and identified the bias generator as a combination of transistors 1050, 1055 and 1060-

1064. The Examiner further contended that the allegedly disclosed method comprised, "providing a metal-programmable transistor [1060, 1064]" and "metal programming (Fig. 10D, 10E) the metal-programmable transistor [1060, 1064] to connect the transistor to circuitry of the bias generator [1050, 1055 and 1060-1064]". The Examiner further contended that Patel et al. disclosed the metal programming, "to modify the available magnitudes of the set (Col. 15 lines 50-55)".

Appellant respectfully disagrees. In particular, Patel et al. fail to disclose, explicitly or implicitly, each element of Claim 21. As is discussed above with respect to Claims 1 and 6, Patel et al. disclose neither a "bias generator" nor a "bias voltage output signal" produced by the bias generator, as defined by Appellant and recited in Claim 21, contrary to the Examiner's contention. Similarly, Patel et al. fail to disclose, "modifying a set of available magnitudes of a bias voltage output signal", as further recited in Claim 21.

That notwithstanding, Patel et al. further do not disclose, "metal programming the [provided] metal-programmable transistor ... to modify the available magnitudes of the set", as recited in Claim 21. As has already been discussed at length above, the only metal programmable transistors disclosed Patel et al. are transistors 1060, 1062, 1064 and 1066. These transistors are disclosed exclusively as means for adjusting or "fine-tuning" an ***input threshold trip point*** of the inverting input buffer, according to Patel et al. However, nowhere in that disclosed by Patel et al. is there mention or even a suggestion that transistors 1060, 1062, 1064 and 1066 can provide any other adjustment or modify any other characteristic of the inverting input buffer circuit beyond the input threshold trip point. Moreover, as discussed above, the disclosed transistors 1060, 1062, 1064 and 1066, associated as they are with the inverting input buffer circuit (i.e., transistors 1050 and 1055) cannot effect any change whatsoever to a magnitude of a signal (e.g., "To Core") produced by the inverting input buffer. As such, Patel et al. do not and respectfully cannot disclose, "metal programming ... to modify the available magnitudes of the set", as recited in Claim 21.

Therefore, the Examiner failed to establish that Patel et al. disclose 'each and every element' of Claim 21 and disclose the claimed elements 'arranged as in the claim' that are recited in Appellant's Claim 21, as required for establishing *prima facie* anticipation. *W.L. Gore & Associates v. Garlock*, cited *supra* and *Lindemann*

Maschinenfabrik GmbH v. American Hoist & Derrick Co., cited *supra*. In particular, as detailed above, the Examiner failed to show that there is, "no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention," as required by the Federal Circuit. *Scripps Clinic & Research Found. V. Genentech Inc.*, cited supra). Hence, a *prima facie* case of anticipation with respect to Claim 21 in view of Patel et al. has not been and respectfully cannot be established.

Claims 22-25 as dependent from Claim 21

Claims 22-25 are ultimately dependent from and include all of the limitations of base Claim 21. Having failed to establish *prima facie* anticipation of base Claim 21 with respect to Patel et al., the Examiner has similarly failed to establish *prima facie* anticipation of Claims 22-25 that are dependent therefrom for at least the same reasons given above regarding Claim 21. In particular, the Examiner has failed to show and properly support that Patel et al. disclose, explicitly or implicitly, at least "bias generator circuitry", such that the Examiner cannot show "metal programming comprises connecting ... to the bias circuitry (Claim 22); such that the recited ON state resistances are combined (Claims 23 and 24); and further comprises "selecting a respective ... transistor and connecting the selected respective ... transistor to the bias generator circuitry" (Claim 25).

For at least the reasons set forth above, Appellant respectfully submits that the Examiner erred in making final the rejection of Claims 1, 3-8, 11 and 21-25 for failing to establish a *prima facie* case of anticipation given the facts in evidence. As such, the final rejection of Claims 1, 3-8, 11 and 21-25 under 35 U.S.C. 102(b) as being anticipated by Patel et al. should have been withdrawn by the Examiner.

<u>**Ground II**: Rejection of Claim 2 under 35 U.S.C. 103(a) as being unpatentable over Patel et al. in further view of Ando</u>

Appellant respectfully submits that the Examiner erred in making final a rejection of Claim 2 under 35 U.S.C. §103(a) as being unpatentable over Patel et al. in further view of Ando for failing to establish and properly support a *prima facie* case of obviousness with respect to the references, as detailed hereinbelow.

Specifically, the Examiner failed to show with respect to the rejected claim ***each of*** 1) "some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings"; 2) "a reasonable expectation of success" in modifying or combining the teachings of the references; ***and*** 3) that the prior art references, "teach or suggest all the claim limitations", as required by the courts for establishing a *prima facie* case of obviousness. MPEP, Section 2142, *Establishing a Prima Facie Case of Obviousness*. Moreover, the Examiner failed to establish that the teaching or suggestion to make the claimed combination and the reasonable expectation of success are both, "found in the prior art, and ***not*** based on applicant's disclosure". *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991) (***emphasis*** added). In short, with respect to a combination of Patel et al. and Ando, the Examiner failed to show the elements necessary for establishing and supporting a *prima facie* case of obviousness consistent with well-established law and a myriad of court decisions.

Claim 2 Standing Alone

In rejecting Claim 2 under 35 U.S.C. 103(a), the Examiner admitted, "Patel et al. ... does not discloses [*sic*] the bias output signal (To Core) is biases [*sic*] a gate of a weak write pull-down transistor of a write drives [*sic*] in the memory (SRAM)". The Examiner contended, "Fig 1 of Ando discloses a bias signal (WW) is biasing a gate of a weak write pull down transistor (1) of a writer [*sic*] driver (WB) in the memory". The Examiner concluded, "it is obvious to use the bias generator of Patel et al. in an environment where a driver of a memory is needed or a general combination of memory system elements to provide a particular end result". The Examiner further suggested, "[o]ne a [*sic*] particular end result is know [*sic*] from the viewpoint of overall memory system," and stated, "it would be obvious to use the particular circuit with specifics [*sic*] components as discussed in Ando to meet refinement for that specific use". The Examiner contended, "[t]his refinement of know [*sic*] circuitry such as that taught in Ando is ***well known*** in the operating and use of memory circuitry ... and is considered to be routine part of the final stages prior to final preparation for sale and end use" (***emphasis*** added). The Examiner's contention

regarding the "well known" nature of refinement was made without providing extrinsic evidence in support of the contention.

Appellant respectfully disagrees. As to a motivation to modify or combine the references, it is consistent with well-established law that, "[o]bviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. 'The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art.' *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Fine*, 837 F.2d 1071, 1075 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992)". MPEP §2143.01 *Suggestion or Motivation to Modify the References.* In particular, as reasoned by the Federal Circuit (*In re Sang Su Lee*, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002)),

> When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness. See e.g., McGinley v. Franklin Sports, Inc., 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001) ("the central question is whether there is reason to combine [the] reference," a question of fact drawing on the Graham factors).
>
> "The factual inquiry whether to combine references must be thorough and searching." Id. It must be based on objective evidence of record. This precedent has been reinforced in myriad decisions, and cannot be dispensed with. See, e.g., Brown & Williamson Tobacco Corp. v. Philip Morris Inc., 229 F.3d 1120, 1124-25, 56 USPQ2d 1456, 1459 (Fed. Cir. 2000) ('a showing of a suggestion, teaching, or motivation to combine the prior art is an 'essential component of an obviousness holding'") (quoting C.R. Bard, Inc., v. M3 Systems, Inc., 157 F.3d 1340, 1352 48 USPQ2d 1225, 1232 (Fed. Cir. 1998)).

Furthermore, according to the Federal Circuit, " 'teachings of references can be combined only if there is some suggestion or incentive to do so' "(emphasis in original). *In re Fine*, cited *supra* (quoting *ACS Hosp. Sys., Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). "[E]ven when the level

of skill in the art is high, the Board [or the Examiner] must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combination. In other words, the Board [or the Examiner] must ***explain the reasons*** one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious" (***emphasis*** added). *In re Rouffet*, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998).

Moreover, "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art ***also suggests the desirability*** of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)" (***emphasis*** added). MPEP §2143.01, cited *supra*. For a motivation to combine/modify to be legitimate and therefore be employed to support a *prima facie* case of obviousness, there must be, "evidence that 'a skilled artisan, ***confronted with the same problems as the inventor*** and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed'" (***emphasis is*** added). *Ecolochem, Inc. v. Southern Calif. Edison Co.*, 227 F.3d 1361, 1375, 56 USPQ2d 1065, 1075 (Fed. Cir. 2000) (quoting *In re Rouffet*, cited *supra*). Therefore, in addition to providing evidence from the prior art to support selecting and combining, the Examiner is required to establish and provide evidence to support the desirability of the combination in light of the problem or problems that faced the inventor.

Regarding Patel et al. and Ando, the Examiner merely states without ***evidentiary support*** that it would be obvious to combine the references based on what appears to be a hypothetical rationale that the Examiner considered 'routine'. However, the Examiner has not and respectfully cannot point to any portion of the respective disclosures of Patel et al. or Ando where such a motivation is at least ***explicitly*** expressed. Thus, the Examiner's motivation to combine/modify the references is clearly not found 'in the references themselves'.

Furthermore, the Examiner provided ***no extrinsic evidence to support*** a contention that a teaching, suggestion, or motivation ***not found explicitly*** in the cited references was ***either present implicitly*** in that taught by the references (which in this instance, clearly it is not) ***or*** was ***in the knowledge generally available to one of ordinary skill in the art***. Specifically, ***the Examiner cited nothing*** (i.e., no extrinsic

evidence) beyond the references themselves in support of the Examiner's motivation. Therefore, the Examiner ***is not*** relying on implicit teachings or general knowledge of the skilled artisan. As such, the Examiner respectfully cannot contend that the Examiner's motivation regarding combining the references are, "found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art", as required by the courts to support *prima facie* obviousness. *In re Kotzab*, cited *supra*.

In addition, the Examiner's motivation lacks that necessary to qualify as a legitimate or supported motivation to combine/modify according to the courts. In particular, the Examiner offered no explanation regarding how the proposed motivation would lead the skilled artisan to select and combine the references, as relied upon by the Examiner for the subject rejection. No explanation is presented regarding "the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them [thereby rendering] the claimed invention obvious". *In re Rouffet*, cited *supra*. In short, the Examiner's motivation fails to address ***why*** a skilled artisan, ***without*** knowledge or benefit of Appellant's teachings, would make the ***specific choice*** to combine Patel et al. and Ando as opposed to some other combination of references.

In addition, the Examiner's motivation provides no insight into why one skilled in the art would have found it obvious to make the particular and specific modification of the relevant teachings of references that the Examiner suggests other than a vague and unsupported statement that it is "well known in operating and use of memory circuitry". Thus, the Examiner's motivation fails to address why the skilled artisan would have been motivated to combine/modify Patel et al. and Ando.

Additionally, the Examiner failed to establish, or for that matter, even attempt to establish, that the prior art or the skilled artisan with ***no knowledge of the claimed invention*** would have: (a) recognized the desirability of the combination/modification proposed by the Examiner, or (b) selected the specific elements from the cited prior art references for combination/modification, as suggested by the Examiner, when confronted with the same problem faced by the inventor. In fact, the Examiner did not explicitly or implicitly consider the problem(s) faced by the inventor as motivation for the combination/modification proposed by the Examiner. Similarly,

the Examiner has not identified specifically the principle of or explained the reasons why the skilled artisan would have been motivated to select and combine the references. *In re Rouffet*, cited *supra*. Hence, the Examiner simply has not provided a legitimate motivation to combine the cited references in support of a *prima facie* case of obviousness.

In fact, Appellant can discern no objective reason for combining/modifying Patel and Ando, as proposed by the Examiner, other than a possible attempt on the part of the Examiner to address acknowledged deficiencies in the disclosure of Patel et al. with respect to Appellant's claim limitations. In other words, the Examiner appears to be improperly using Appellant's teaching as a blue print for picking and choosing among the disclosed features of the cited references. The Examiner may not, "resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in its factual basis". *In re Warner*, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied 389 U.S. 1057 (1998).

The Federal Circuit held, "[i]t is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious ... '[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to depreciate the claimed invention.'" *In re Fritch*, 972 F. 2d 1260, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992), quoting *In re Fine*, cited *supra*. The Federal Circuit has repeatedly and clearly warned against, "the insidious effect of a hindsight syndrome wherein that which only the invention taught is used against its teacher". *In re Kotzab*, cited *supra* (citing *W.L. Gore & Assocs., Inc. v. Garlock, Inc.*, cited *supra*). ("To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the invention taught is used against its teacher", *W.L. Gore & Assocs., Inc. v. Garlock, Inc.* cited *supra*.) As stated by the Federal Circuit, "Obviousness ***may not*** be established using hindsight" (***emphasis*** added). *Para-Ordnance Mfg. v. SGS Importers Int'l*, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995). "Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together

the prior art to defeat patentability—the essence of hindsight". *In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

In sum, the Examiner's motivation with respect to the combination/modification of Patel et al. in view of Ando essentially fails to meet ***any*** of the requirements for a legitimate suggestion or motivation to combine/modify, as expressed by the courts. Instead, as outlined above, the Examiner's motivation to combine/modify Patel et al. and Ando is fatally flawed. As such, the *prima facie* case of obviousness with respect to the rejection of Claim 2 is defeated at least for lack of a legitimate suggestion or motivation to combine/modify the references according to the Federal Circuit. See *In re Sang Su Lee*, cited *supra*. Furthermore, given the lack of a supported, legitimate motivation to combine the respective references, ***any*** consideration regarding what the respective combination may or may not disclose is moot.

The Examiner also failed to show and was silent on there being a reasonable expectation of success in modifying the teachings of Patel et al. with the teachings of Ando. The Examiner is obliged to show that such a reasonable expectation of success exists according to the case law. As provided by the Federal Circuit, the Examiner must establish that the reasonable expectation of success, as well as the teaching or suggestion to make the claimed combination, are both "found in the prior art, and **not** based on applicant's disclosure". *In re Vaeck*, cited *supra*. The Examiner is not at liberty to dispense with this requirement in establishing a *prima facie* case of obviousness under 35 U.S.C. 103.

Notwithstanding the lack of a supported motivation to combine/modify and the lack of a showing of a reasonable expectation of success in the combination, the combination of Patel et al. and Ando also fails to disclose or suggest ***all*** of the claim limitations of Claim 2. Claim 2 is dependent from and includes all of the limitations of base Claim 1. The combination of the references fails to disclose or suggest at least all of the limitations recited separately in e base Claim 1. For example, Patel et al. combined with Ando at least fail to disclose one or more of a "bias generator", "an output of the bias generator", and "means for adjusting a set of available magnitudes of a bias voltage output signal at the output using metal programming".

With respect to Claim 2 standing alone , the combination of Patel et al. and Ando further fail to disclose or suggest, "wherein the bias voltage output signal biases

a gate of a weak write pull-down transistor of a write driver in the SRAM with a target magnitude predetermined for the SRAM". For example, neither Patel et al. nor Ando disclose or suggest, "a weak write pull-down transistor", as recited in Claim 2. Contrary to that contended by the Examiner, the reference to "WW" in Ando is to a "write word signal" (Col. 3, lines 10-11). Such a "write word signal" is unrelated to "the bias voltage output signal" that "biases a gate of a weak write pull-down transistor of a write driver ...", as recited in Claim 2. Moreover, Patel et al. and Ando, whether considered separately or together, neither mention nor suggest a "write driver in the SRAM" or that there may be "a target magnitude [of the bias] predetermined for the SRAM", as recited in Claim 2. In fact, the disclosure of Ando is entirely directed to a capacitorless DRAM gain cell and does not even mention or consider SRAM.

As such, contrary to the Examiner's contention, the combination of Patel et al. and Ando fails to disclose or suggest all of the limitations of Claim 2, as required by the courts for establishing and supporting *prima facie* obviousness. See *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). As with a failure to provide a legitimate motivation to combine and separately, a reasonable expectation of success, a failure by the Examiner to establish that the combined references disclose or suggest all of the limitations of Claim 2 further defeats *prima facie* obviousness. *In re Royka*, cited *supra*.

For at least the reasons set forth above, Appellant respectfully submits that the Examiner erred in making final the rejection of Claim 2 for failing to establish a *prima facie* case of obviousness given the facts in evidence. As such, the final rejection of Claim 2 under 35 U.S.C. 103(a) over Patel et al. in view of Ando should have been withdrawn by the Examiner.

Summary

As presented above, the Examiner failed to establish a *prima facie* case of anticipation of any of Claims 1, 3-8, 11 and 21-25 under 35 U.S.C 102(b) in view of Patel et al. and further failed to establish a *prima facie* case of obviousness of Claim 2 under 35 U.S.C. 103(a) over Patel et al. in further view of Ando. Hence, Claims 1-8, 11 and 21-25 are separately patentable, as provided above. As stated by the Federal Circuit, "if the examination at the initial stage does not produce a *prima facie* case of

unpatentability, then without more the applicant is entitled to grant of patent". *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). Accordingly, Appellant respectfully requests that the Board of Patent Appeals and Interferences reverses the rejection of Claims 1, 3-8, 11 and 21-25 under 35 U.S.C. 102(b) and the rejection of Claim 2 under 35 U.S.C. 103(a), and further allows Claims 1-8, 11 and 21-25.

Respectfully submitted,
BLAINE STACKHOUSE ET AL.

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date shown below.

_____ 7/6/06
J. Michael Johnson Date

CLAIMS APPENDIX

Listing of Claims on Appeal

Claim 1: A bias generator for testing of a static random access memory (SRAM) comprising:

an output of the bias generator; and

means for adjusting a set of available magnitudes of a bias voltage output signal at the output using metal programming.

Claim 2: The bias generator of Claim 1, wherein the bias voltage output signal biases a gate of a weak write pull-down transistor of a write driver in the SRAM with a target magnitude predetermined for the SRAM.

Claim 3: The bias generator of Claim 1, wherein the means for adjusting comprises a metal-programmable transistor in the bias generator, the metal-programmable transistor comprising either or both of a metal-programmable pull-up transistor and a metal-programmable pull-down transistor that change one or both of a range and a resolution of the set of available magnitudes when the metal-programmable transistor is metal programmed.

Claim 4: The bias generator of Claim 3, further comprising:

a pull-up array of transistors connected between a first supply voltage and the bias generator output;

a pull-down transistor connected between the bias generator output and a second supply voltage; and

a gate bias circuit connected between a mode select input and a gate of the pull-down transistor,

wherein the metal-programmable pull-up transistor is connectable in parallel or in series with the pull-up transistor array, and

wherein the metal-programmable pull-down transistor is connectable in parallel or in series with the pull-down transistor.

Claim 5: The bias generator of Claim 4, wherein each of the metal-programmable pull-up transistor and the metal-programmable pull-down transistor has a respective ON state resistance that, when either or both are metal programmed, combines with an effective ON state resistance of the pull-up transistor array and an ON state resistance of the pull-down transistor to adjust the set of available magnitudes.

Claim 6: A bias generator for testing of a static random access memory (SRAM) comprising:

a metal-programmable transistor that adjusts a set of available magnitudes of a bias voltage output signal at the bias generator output when metal programmed.

Claim 7: The bias generator of Claim 6, further comprising:

a pull-up array of transistors connected between a first supply voltage and the bias generator output;

a pull-down transistor connected between the bias generator output and a second supply voltage; and

a gate bias circuit connected between a mode select input and a gate of the pull-down transistor,

wherein the metal-programmable transistor is connectable one or both of in series and in parallel with either or both of the pull-up array and the pull-down transistor.

Claim 8: The bias generator of Claim 6, wherein the metal-programmable transistor comprises either or both of a metal-programmable pull-up transistor and a metal-programmable pull-down transistor, the metal-programmable transistor changing one or both of a range and a resolution of the set of available magnitudes when metal programmed.

Claim 11: The bias generator of Claim 7, wherein the pull-up array transistors are p-type metal oxide semiconductor (PMOS) transistors that function to pull up the bias voltage output signal when in an ON state, and

wherein the pull-down transistor is an n-type metal oxide semiconductor (NMOS) transistor that functions to pull down the bias voltage output signal to the second supply voltage when in the ON state, the second supply voltage being less than the first supply voltage, the second supply voltage optionally being zero volts or a ground voltage.

Claim 21: A method of modifying a set of available magnitudes of a bias voltage output signal generated by a bias generator comprising:

providing a metal-programmable transistor in the bias generator; and

metal programming the metal-programmable transistor to connect the transistor to circuitry of the bias generator, such that a corresponding ON state resistance of the metal-programmed transistor is combined with an effective ON state resistance of the circuitry to modify the available magnitudes of the set.

Claim 22: The method of modifying of Claim 21, wherein providing a metal-programmable transistor comprises providing either or both of a metal-programmable pull-up transistor and a metal-programmable pull-down transistor in the bias generator, and

wherein metal programming the metal-programmable transistor comprises connecting either or both of the metal-programmable pull-up transistor and the metal-programmable pull-down transistor to the bias generator circuitry.

Claim 23: The method of modifying of Claim 22, wherein metal programming the metal-programmable pull-up transistor to connect to the circuitry combines a corresponding pull-up ON state resistance of the metal-programmed pull-up transistor with an effective ON state resistance of a pull-up transistor array of the bias generator circuitry.

Claim 24: The method of modifying of Claim 22, wherein metal programming the metal-programmable pull-down transistor to connect to the circuitry combines a corresponding pull-down ON state resistance of the metal-programmed pull-down transistor with an ON state resistance of a pull-down transistor of the bias generator circuitry.

Claim 25: The method of modifying of Claim 22, wherein providing a metal-programmable transistor comprises providing either or both of a selection of metal-programmable pull-up transistors and a selection of metal-programmable pull-down transistors in the bias generator, at least one of the metal-programmable transistors of each respective selection being different from other metal-programmable transistors of the respective selections, and

wherein metal programming the metal-programmable transistor comprises selecting a respective metal-programmable transistor from either or both the pull-up transistor selection and the pull-down transistor selection, and connecting the selected respective metal-programmable transistor to the bias generator circuitry.

EVIDENCE APPENDIX

There is no evidence submitted pursuant to 37 CFR §§ 1.130, 1.131, 1.132 or any other evidence entered by the examiner that is relied upon by Appellant.

RELATED PROCEEDINGS APPENDIX

Not Applicable.

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